Clock Source Module
p/n L-6001-CLK20-3

DESCRIPTION

Clock source

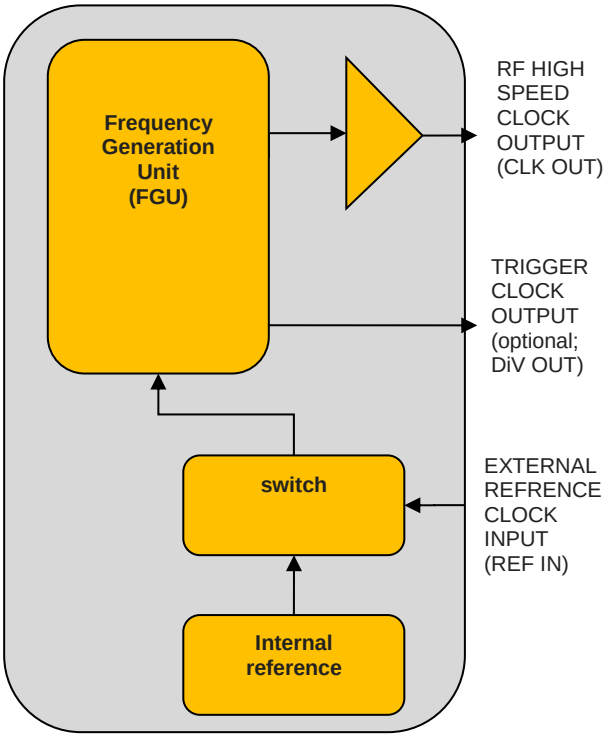
CLK20 is a clock source module that plugs into the PARALLEX® chassis. The clock works over a continuous range from 78.125 MHz to 20 GHz. Functionally it is not bound to the EBERT modules hence it can be used for driving any other devices, too. It has a divided clock output to offer a subrate trigger for oscilloscopes that have limited trigger bandwidth.

CLOCK SOURCE MODULE
p/n L-6001-CLK20

KEY FEATURES

- internal or external reference clock generator
- clock multiplier function
- optional jitter insertion
- output voltage 200...600 mV
- clock output 78.125MHz to 20GHz
- trigger clock output 78.125MHz to 5GHz
- single ended output
- GPIB/LAN/USB Interface via PARALLEX® chassis
- Small size: width 25.4mm (1”)

FUNCTIONAL BLOCK DIAGRAM



PARALLEX® PLATFORM: LETS YOU START SMALL AND GROW LATER

PARALLEX® is a low-cost, modular Bit Error Rate Test Platform used for verification and test of optical and electrical components, sub-assemblies and systems at 1 to 29 Gbps. PARALLEX® allows users to perform several BER tests simultaneously using a single clock source. The system is ideal for parallel interfaces or multiple independent interfaces. PARALLEX® is scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the PARALLEX® system’s scalability to perform parallel testing in volume production environments.

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KEY PERFORMANCE PARAMETERS

RF HIGH SPEED CLOCK OUTPUT

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
RF-clock frequency full range	$f_{RFoutUncal}$	0.078125		20	GHz	
RF-clock frequency calibrate power range	$f_{RFoutCal}$	0.078125		15	GHz	
RF-clock frequency step	$f_{RFoutStep}$		10		Hz	
RF-clock output voltage (10GHz-15GHz)	V_{RFout}	200		600	mV	±300mV
RF-clock output power (10GHz-15GHz)	P_{RFout}	-10		0	dBm	±3dBm
RF-clock output voltage (78.125MHz-10GHz)	V_{RFout}	200		1200	mV	±300mV
RF-clock output power (78.125MHz-10GHz)	P_{RFout}	-10		6	dBm	±3dBm
RF-clock output power step	$P_{RFoutStep}$		1		dB	±2dB
RF-clock output termination			AC - coupled			
RF-clock output duty cycle	$t_{RFoutDC}$	45		55	%	
RF-clock output impedance	$Z_{RFoutRef}$	45		55	Ω	
RF-clock rise and fall time	t_r / t_f	15		35	ps	20% - 80%
RF-clock phase jitter rms	RJ_{RFout}		200 200	300 400	fs_{rms}	50KHz – 80MHz 10Hz – 100Hz
F-clock output phase noise	PN_{RFout}			-44dBc -76dBc -90dBc -84dBc -96dBc -99dBc -126dBc -142dBc	10Hz 100Hz 1KHz 10KHz 100KHz 1MHz 10MHz 100MH	At 12.5GHz operating frequency

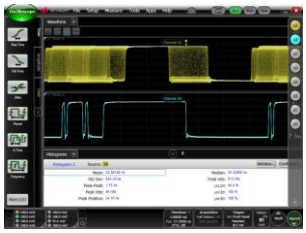
Option 161

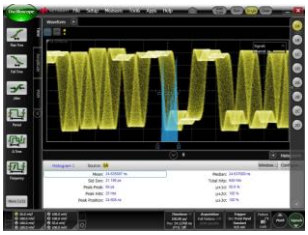
This option add sinusoidal jitter capability

PARAMETER	SYMBOL	min	TYP	Max	UNIT	NOTE
Jitter modulation frequency	f_{mod}	1000		$80*10^6$	Hz	
Jitter modulation amplitude	J_{pp}	0.01		17	UI	1)
REF OUT No Jitter Added	$f_{refclean}$	78.125		156.25	MHz	

Notes

1) Depends on chosen pattern generator. Assuming a data rate of 10.0Gb/s then 17UI = 17/10GHz = 1.7ns, and smallest adjustable jitter is at 28Gb/s at 14GHz clock source 0.01UI = 350fs.





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