Error Detector Module

PN L-6001-EED10-6

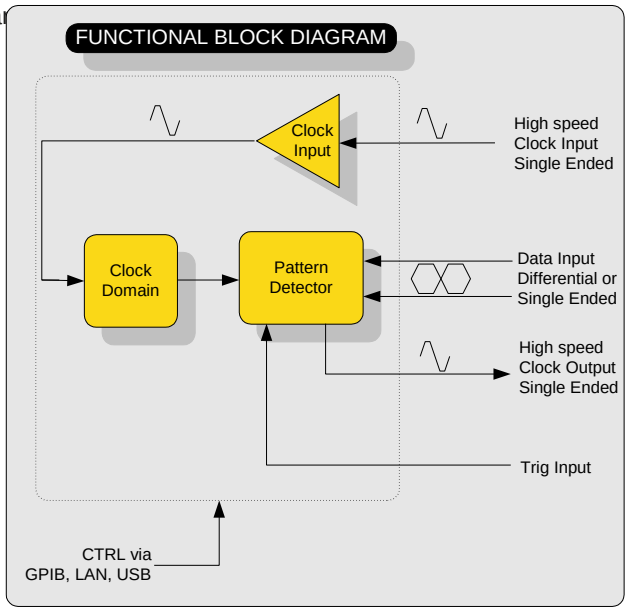
DESCRIPTION

EED10-6 is an Electrical Error Detector module that plugs into the *XBERT* and *Parallex*® Chassis. EED10-6 can receive electrical data from 2 Gbps up to 13 Gbps, optionally up to 14.5G. Front panel indicators give immediate status for Rx Data.

ERROR DETECTOR MODULE PN L-6001-EED10-6

KEY FEATURES

- Data Rates 2 to 13Gbps
- Optional operation up to 14.5G
- Optional differential input
- Differential Electrical Error Detector (SMA connector)
- PRBS: 7, 9, 10, 11, 15, 21, 23, 31
  User-Pattern: 8Bit - 64Kbit
  Clock-Pattern: $^1/_1$, $^1/_2$, $^1/_4$, $^1/_8$
  Additional: K28.0-K28.7, CJPAT, SSPS-64 ar
- Data input polarity swap
- External gating Input
- Automatic data alignment routine
- BER Detection: 0.5 to <1E-15
- Data log Gating-time: up to 5000h
- High speed Clock Input and Output
- LabView™ drivers available
- GPIB/LAN/USB Interface via XBERT Chassis.
- Small size: width 25.4mm (1”)



XBERT PLATFORM: LETS YOU START SMALL AND GROW

XBERT is a low-cost, modular Bit Error Rate Test Platform used for verification and test of up to 13Gbps optical and electrical chip, sub assembly and system designs. *Parallex*® allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. *XBERT* and *Parallex*® are scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the *XBERT* and *Parallex*® system’s scalability to perform parallel testing in volume production environments.

EED10-6 Module Product Overview

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KEY PERFORMANCE PARAMETERS

PRELIMINARY

PARAMETER	SYMBOL	Min	Max	UNIT	NOTE
Data Rate	DR	2	13	Gbps	Option144 for Max 14.4Gbps
Data Formats			NRZ		
PRBS Pattern			7, 9, 10, 11, 15, 21, 23, 31		
User-Defined Pattern length		8	65536	Bit	
Measurable Bit Error Rate	BER	<1E-15	0.5		
Data Input Signal Amplitude	$D_{InP/N}$	100	1000	mV_{pp}	
Differential Data Input signal ($D_{InDiff}=D_{InP}-D_{InN}$)	D_{InDiff}	200	2000	mV_{pp}	Option 147 for differential input
External gating input	Gi				Starts and stops the gating measurement
Single ended Data Input Impedance	Z_{Ise}	45	55	Ω	
Data Input Termination			AC -coupled		
Clock Input Amplitude		300	1000	mV_{pp}	
Clock Output Amplitude		300	1000	mV_{pp}	Not adjustable
Clock Input / Output Frequency	F_{Clk}	1	13	GHz	
Clock Input / Output Impedance	Z_{Clk}	45	55	Ω	
Clock Input / Output Termination			AC - coupled		
Operating Temperature	T_{OP}	0	40	°C	Ambient temp.

EED10-6 Module Product Overview

Am Borsigturm 13
13507 Berlin-Germany
+49 30 814 512 40 00 ph
+49 30 814 512 40 20 fax
www.luceotec.com
sales@luceotec.com

LUCEO TECHNOLOGIES